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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,074	01/30/2004	Nobuyuki Minowa	1309.43464X00	6113

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EXAMINER	
KRAVETS, LEONID	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/767,074	MINOWA, NOBUYUKI	
	Examiner	Art Unit	
	Leonid Kravets	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 10-23* is/are rejected.

7)☒ Claim(s) *7-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *Four IDSs*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 2003-396786, filed on November 27, 2003.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

3. Claim 1 is objected to because of the following informalities: In lines 7 and 13, the limitation reads and/or. This is improper claim language. In line 9, "an address map memory means for storing a first address map **on** which the first local memory addresses for each of said one or more first processors are recorded" should read, "an address map memory means for storing a first address map **in** which the first local memory addresses for each of said one or more first processors are recorded".

4. Claims 21 and 22 are also objected because the limitation reads and/or reads read information

5. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 3 recites the limitation "the second local memory write address" in line 18. There is insufficient antecedent basis for this limitation in the claim. There is unclear antecedent basis for the second local memory write address acquired on the target second processor.

8. Claim 15 recites the limitation "the relay device selectively performs an operation of this transfer after the write information has been temporarily stored in the relay memory, and an operation of this transfer without storing the write information in the relay memory. It is impossible to both store and not store the write information.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1, 3-5, 10, 12-13, 16, 18, 20-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Glasco et al. (Pub No. 2003/0225909).

11. As per claim 1, Glasco teaches an information processing device which processes information using a plurality of processors (Abstract) comprising:

One or more first processors that have one or a plurality of first local memories [Glasco states a processor cluster can include a memory subsystem comprising memory banks (Paragraph 19)]; and

One or more second processors which directly write write information into a target first local memory that a target first processor selected from among said first processors has, and/or which directly read read information from said target first local memory [Glasco describes a read sent from one local home cluster to a different home cluster, while the read operation is described, a write operation can be inferred from the description (Paragraphs 58 and 59)]; and.

An address map memory means for storing a first address map on which the first local memory addresses for each of said one or more first processors are recorded (Paragraph 42), wherein each of said one or more second processors acquires the first local memory address of said target first processor from said first address map (Figure 5), writes said write information into the acquired first local memory address, and/or reads said read information from the acquired first local memory address (Paragraphs 58 and 59).

12. As per claim 3, Glasco describes the information processing device according to claim 1, further comprising

One or a plurality of second local memories belonging to each of said one or more processors [each memory cluster has the structure of claim 1 (Paragraph 19)],

A first address map memory means for storing a first address map on which the first local memory addresses for each of said one or more first processors are recorded (Paragraph 42); and

A second address map memory means for storing a second address map on which second local memory addresses for each of said one or more second processors are recorded [Note each processor cluster has such a memory map (Paragraph 42)];

Wherein a target second microprocessor selected from among said one or more second processors acquires a first local memory write address indicating where writing is to be performed in said target first local memory from said first address map (Paragraph 58), and writes write information into said acquired first local memory address (Paragraph 61), and

When said write information that has been written into said first local memory write address is a read command, said target first processor, in response to said read command, acquires the second local memory write address on the target second processor that originated said read command from said second address map [Responses are mapped from the local tag space back to the global tag space using a table lookup in interconnection controller's pending buffer (Paragraph 61)], reads out information in said first local memory, and writes said information into said acquired second local memory write address [Process is understood to be essentially reversed as that of the writing a read operation above (Paragraph 61)].

13. As per claim 4, Glasco teaches the information processing device according to claim 1, further comprising a relay device which receives said write information from said one or more second processors and transfers the write information to said target first processor (Paragraph 33), wherein said relay device comprises a relay memory [Each node in a processor cluster has a memory space (Paragraph 38)], and when transferring said write information, said relay device selectively performs an operation of said transfer after said write information is temporarily stored in said relay memory [Interconnection controller has a pending buffer (Paragraph 64)], or an operation of said transfer without storing said write information in said relay memory

14. As per claim 5, Glasco discloses the information processing device according to claim 4, further comprising one or a plurality of first devices that have said one or more first processors, wherein said relay device further comprises one or a plurality of transmitting parts which are respectively connected to the said one or a plurality of first devices [Each processor has an interconnect structure (Paragraph 33), and which respectively transmit the received write information to said one or a plurality of first devices and wherein when write information received from a certain second device is to be transmitted to the target first device that has said target first processor, if the target transmitting part that is to transmit this write information is not in a busy state, the received write information is transmitted to the target first device from said target transmitting part without being stored in the relay memory, while if said target

transmitting part is in a busy state, the write information is temporarily stored in the relay memory, and this write information is read out from the relay memory and transmitted to said target first device from the target transmitting part when the busy state of said target transmitting part is released. [The interconnect device has a pending buffer (Paragraph 64)].

15. As per claim 10, Glasco discloses the information processing device according to claim 1, further comprising:

One or a plurality of first devices that have said one or more first processors (Fig 1A, 101):

One or a plurality of second devices that have said one or more second processors (Fig A, 105); and

A relay device that relays said write information from said second devices to said first device that has the target first processor [Switch (Fig 1B, 131) and interconnection controller (Paragraph 19)].

Wherein said relay device has one or a plurality of transmitting parts that respectively transmit information to said one or a plurality of first devices, and one or a plurality of receiving parts that respectively receive information from said one or a plurality of second devices, [Interconnection controller communicates with both processors 202 a-d (local processors) as well as remote clusters (Paragraph 21)] and each of said one or a plurality of transmitting parts and each of the said one or a plurality of receiving parts operate independently of each other [The interconnection

controllers are located within each operating cluster, thus operating independently (Paragraph 5)]

16. As per claim 12, Glasco discloses the information processing device of claim 1, further comprising a relay device which receives said write information including the local memory address of the target first processor from said one or more second processors (Paragraph 58), and transfers this write information to said target first processor [(local interconnection controller forwards request to an interconnection controller in a home cluster (Paragraph 58)], wherein each of said one or more second processors is connected via the relay device so as to be able to respectively communicate with said one or more first processors by one or more logical or physical paths [Interconnection devices route requests from one cluster to another cluster (Paragraph 58)], the relay device stores one or more local memory addresses respectively corresponding to said one or more paths for each second processor [the mapped request is stored in the pending buffer of interconnection controller (Paragraph 58)], and when transferring said received write information, a target path corresponding to said local memory address contained in said received write information is specified, and the write information is transferred to said target first processor via the specified target path [The request of Glasco is forwarded through a path from one cluster to another using interconnection controllers that create a route map (Paragraphs 58 and 59)].

17. As per claim 13, please see rejection of claim 1 above.

18. As per claim 16, please see rejection of claim 5 above.

19. As per claim 18, Glasco discloses the memory control device according to claim 14, wherein said relay device comprises one or a plurality of transmitting pads that respectively transmit information to said one or a plurality of first devices [Interconnection processor of each cluster (Paragraph 5)], and one or a plurality of receiving pads that respectively receive information from said one or a plurality of second devices, each of said one or a plurality of transmitting parts and each of said one or a plurality of receiving pads operate independently from each other [Interconnection processor of each cluster (Paragraph 5)].

20. As per claim 20, please see rejections of claims 1 and 2 above. Claim 20 is rejected for similar reasons.

21. As per claim 21, Glasco discloses an information processing method which processes information using a plurality of processors, comprising the steps in which:

Each of one or more second microprocessors acquires a local memory address of a target first processor from an address map on which local memory addresses for

each of one or more first processors having one or a plurality of local memories are recorded (Paragraph 58); and

Each of said one or more second processors writes write information into said acquired local memory address, and/or reads read information from said acquired local memory address [Process of sending a request from one processor cluster to another processor cluster and receiving a response is described (Paragraphs 58 and 59)].

22. As per claim 22, please see rejections of claims 1 and 4 above.

23. As per claim 23, please see rejections of claims 1 and 4 above. Claim 23 is rejected for similar reasons.

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

26. Claims 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glasco as applied to claim 4 above, and further in view of Adams et al (US Patent 6,124,878).

As per claim 6, Glasco discloses the information processing device according to claim 4, wherein one or more write information storage regions respectively corresponding to one or more transmission sources or transmission destinations of the write information are provided in said relay memory, when temporarily storing the received write information in the relay memory, the relay device stores this write information in the target write information storage region corresponding to the transmission source or transmission destination. Glasco does not disclose that if the amount of information accumulated in said target write information storage region exceeds a first threshold value, a notification of exceeding the first threshold value, which indicates that this threshold value has been exceeded, is transmitted to a specified second device, and the second device that receives said notification of exceeding the first threshold value reduces the frequency with which write information is issued or the amount of write information that is issued to said target local memory or said target first processor.

Adams discloses that if the amount of information accumulated in the write information storage region exceeds a first threshold value, a notification of exceeding the first threshold value, which indicates that this threshold value has been exceeded, is

transmitted to a specified second device, and the second device that receives said notification of exceeding the first threshold value reduces the frequency with which write information is issued or the amount of write information that is issued to said target local memory or said target first processor (Col 2, lines 62-67). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the threshold handling of Adams into the system of Glasco, since Glasco and Adams form the same field of endeavor, namely data transfer and this would allow for better data traffic control.

As per claim 17, please see rejection of claim 6 above.

27. Claims 11, 14, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glasco as applied to claim 1 above, and further in view of Casamatta, (EP 0 908 825)

As per claim 11, Glasco discloses the information processing device according to claim 1. Casamatta discloses one or more local storage regions respectively corresponding to said one or more second processors are provided in the local memories of each of said one or more first processors (Paragraph 53 and 54), Glasco further discloses each of said one or more second processors stores an address map on which the local memory address of said local storage region corresponding to this second processor is recorded for each first processor, and when the write information is

written into the local memory of the target first processor, the local memory address corresponding to this target first processor is acquired from said address map (Paragraph 42), and the write information is written into this acquired local memory address [In the Casamatta and Glasco systems, as in all systems, the write information is written into the acquired local memory address].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the local storage regions of Casamatta into the system of Glasco, since Glasco and Casamatta form the same field of endeavor, namely memory management and this would provide data coherence without burdening the system (Casamatta, Paragraph 19).

As per claim 14, Glasco discloses the memory control device according to claim 13, further comprising:

one or a plurality of first devices in which said one or more first microprocessors are mounted [Processor Cluster (Fig 1B, 123)];

one or a plurality of second devices in which said one or more second microprocessors are mounted [Processor Cluster (Fig 1B 121)]; and

a relay device which relays communications between said one or a plurality of first devices and said one or a plurality of second devices [Switch (Fig 1b, 131)];

Casamatta discloses that one or more local storage regions that respectively correspond to said one or more second microprocessors are provided in said first local memories,

Glasco further discloses the first local memory addresses of the one or more local storage regions that respectively correspond to said one or more first microprocessors are recorded on said first address map (Paragraph 42), each of said one or more second microprocessors can be connected via the relay device so as to be able to respectively communicate with said one or more first microprocessors by one or more logical or physical paths (Fig 1B), and furthermore, when outputting said write information, the second microprocessors acquire the first local memory address of the first local storage region corresponding to said target first processor from said first address map (Paragraph 58), and output write information which has first transmission destination information that includes said acquired first local memory address (Paragraph 58), the relay device stores one or more sets of second transmission destination information that respectively correspond to said one or more paths, and when transferring the received write information, the relay device specifies the target path based on said first and second transmission destination information (Paragraph 58), and transmits the write information to said target first device via the specified target path (Paragraph 58), and the target first device writes the write information received from the relay device into the first local memory address that is included in the write information (Paragraph 59).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the local storage regions that respectively correspond to said one or more second microprocessors provided in said first local memories of Casamatta into the system of Glasco, since Glasco and Casamatta form

the same field of endeavor, namely memory management and this would provide data coherence without burdening the system (Casamatta, Paragraph 19).

As per claim 19, Glasco discloses the memory control device according to claim 18, wherein said relay device comprises a receiving buffer. Glasco does not disclose that the receiving buffer is separate from said relay memory, each of said one or a plurality of receiving pads once store the write information received from said second devices in this receiving buffer.

Casamatta discloses such a separate receiving buffer. In the system of Casamatta, a local memory directory accessible for reading and writing by the controller is provided, further a remote cache tag memory is connected for reading and writing in order to recognize the blocks of data held in the remote cache...and for access both to the remote cache and to the local memories of the other nodes (Paragraphs 60-63).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the separate receiving buffer of Casamatta into the system of Glasco, since Glasco and Casamatta form the same field of endeavor, namely memory management and this would speed up relation of data blocks belonging to the local memory spaces of the other nodes (Casamatta, Paragraph 62).

Allowable Subject Matter

28. Claims 7-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

29. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Frisch (US Patent 5,598,568) discloses a multicomputer with each node having a processor and memory, and crossbars, in which a plurality of communication paths can be established between and among the processing nodes by one or more crossbars, a memory map system by which one node can assess directly the memory of another through the crossbars.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Kravets whose telephone number is 571-272-2706. The examiner can normally be reached on M-F, 8-4:30.

32. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached at (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

33. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

L. K.
Leonid Kravets
Patent Examiner
Art Unit 2189

BEHZAD JAMES PEIKARI
PRIMARY EXAMINER

August 12, 2005